US 20060071883A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2006/0071883 A1**

Oh (43) **Pub. Date: Apr. 6, 2006**

(54) **ELECTRO-LUMINESCENCE DISPLAY DEVICE AND DRIVING METHOD THEREOF**

(75) Inventor: **Du Hwan Oh**, Cheongju-si (KR)

Correspondence Address:
BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, IL 60610 (US)

(73) Assignee: **LG PHILIPS LCD CO., LTD.**

(21) Appl. No.: **11/168,951**

(22) Filed: **Jun. 28, 2005**

(30) **Foreign Application Priority Data**

Oct. 6, 2004 (KR) P2004-079539

Publication Classification

(51) **Int. Cl.**
G09G 3/30 (2006.01)

(52) **U.S. Cl.** **345/76**

(57) **ABSTRACT**

An electro-luminescence display device includes a plurality of column lines, a plurality of first row lines and a plurality of second row lines. The plurality of first row lines cross the column lines and a first scan signal is supplied thereto. The plurality of second row lines intersects the column lines and a second scan signal is supplied thereto. Organic light emitting devices are formed at pixel areas which are defined by the column lines and the first and second row lines. At least two drive switches operate to drive the organic light emitting devices. The second scan signal applies later than the first scan signal to activate the drive switches. A kick-back voltage is generated upon a voltage change of the first row line. A kickback compensation circuit operates to cancel the kickback voltage.

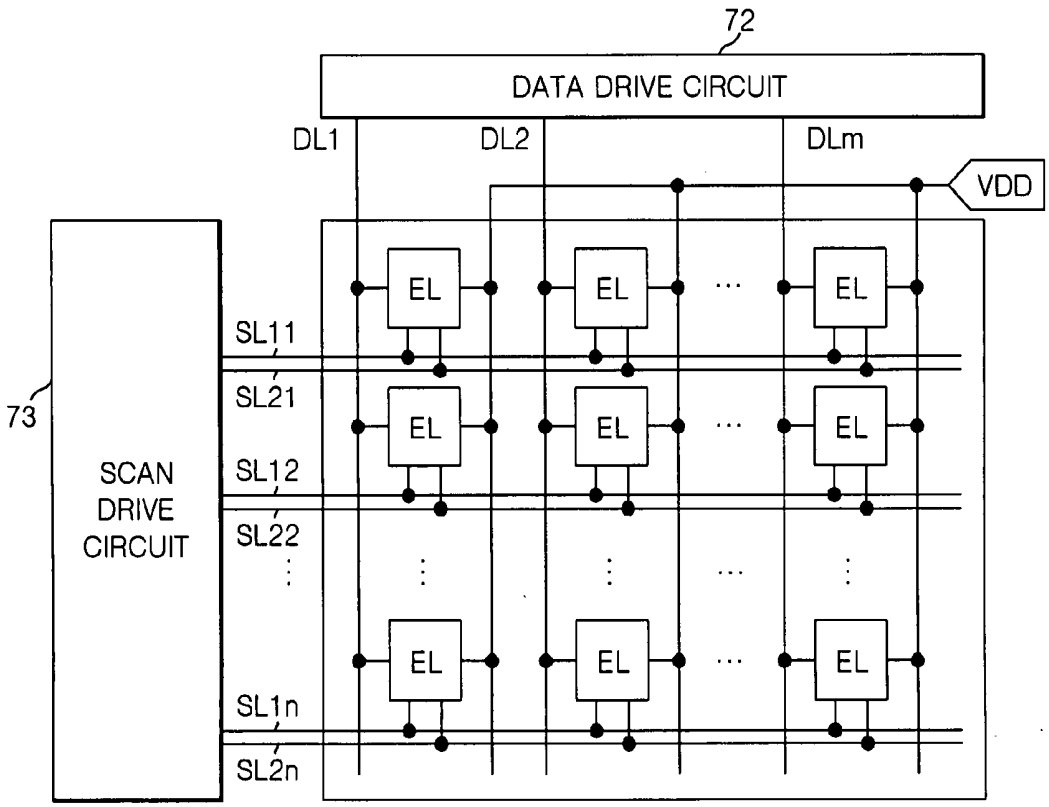


FIG. 1
RELATED ART

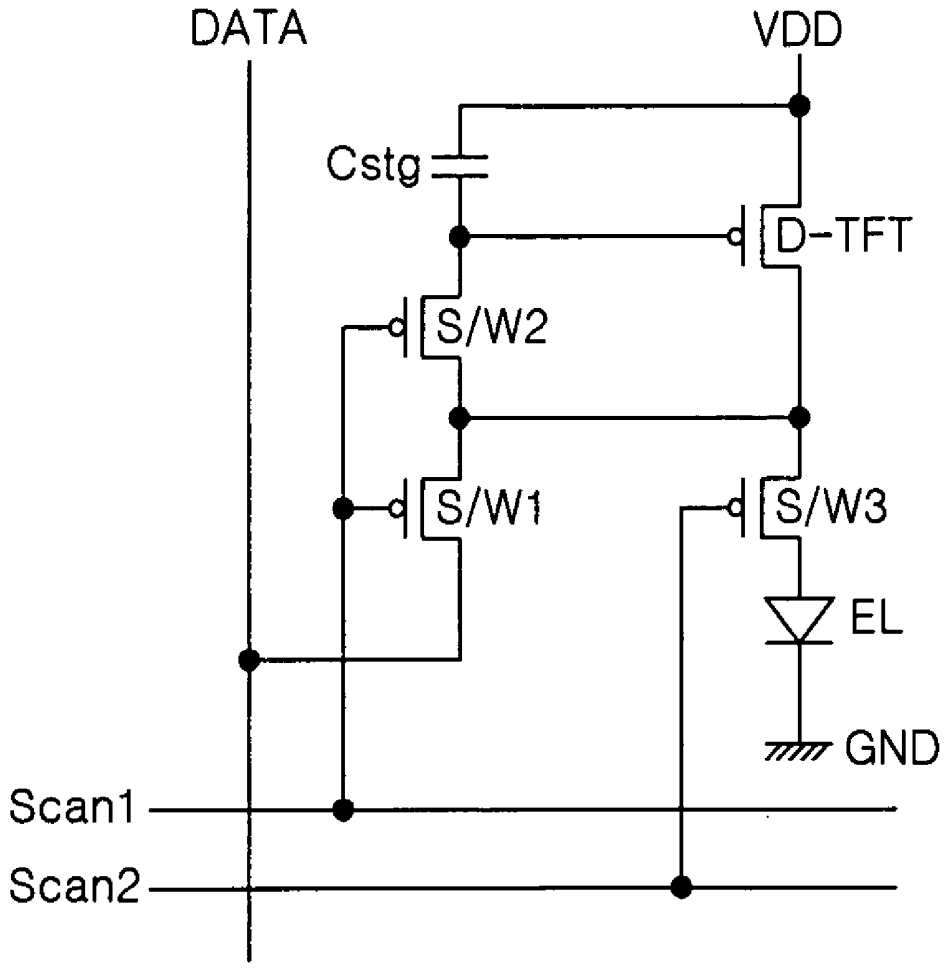


FIG.2
RELATED ART

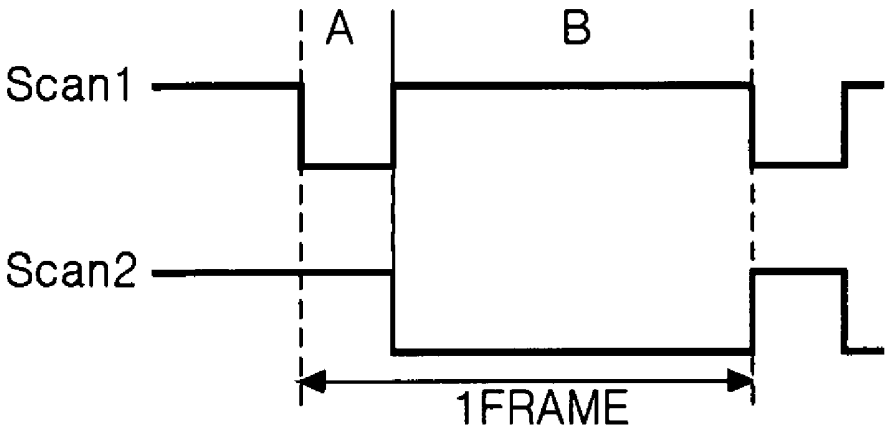


FIG.3
RELATED ART

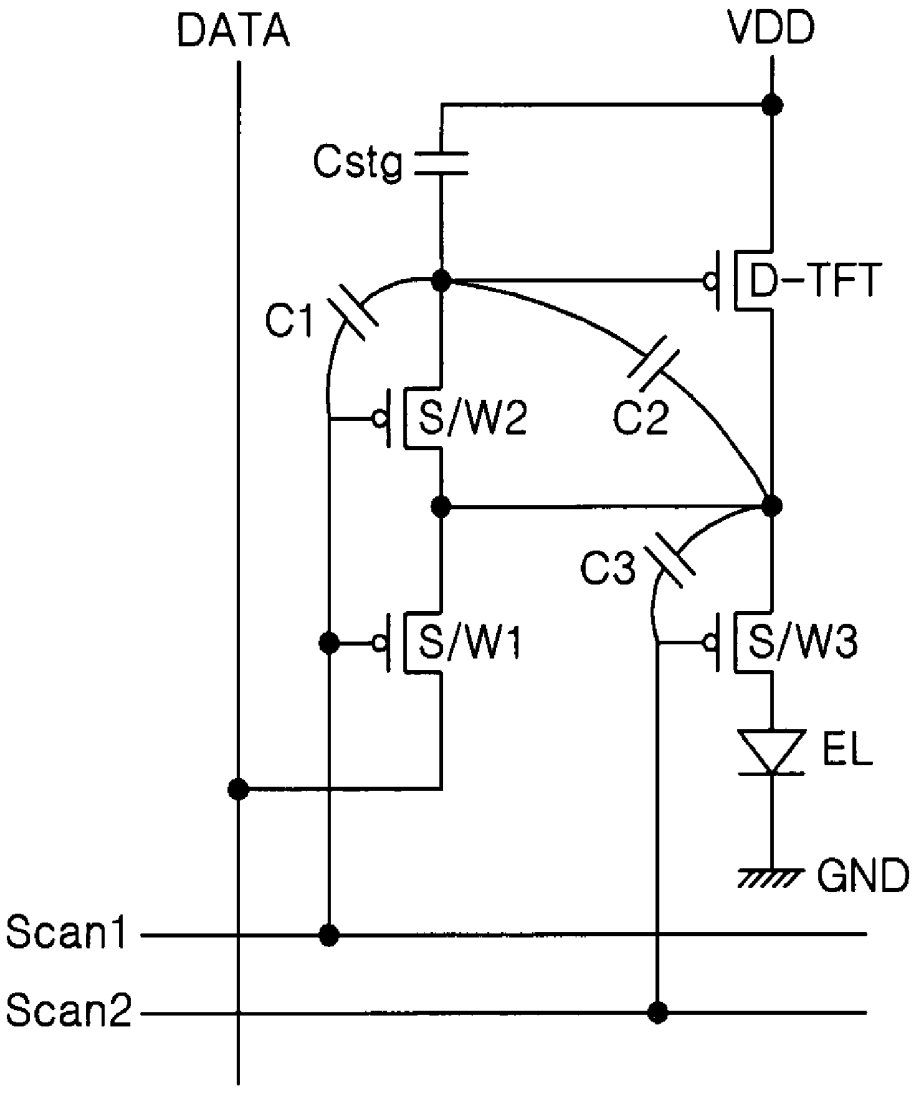


FIG. 4
RELATED ART

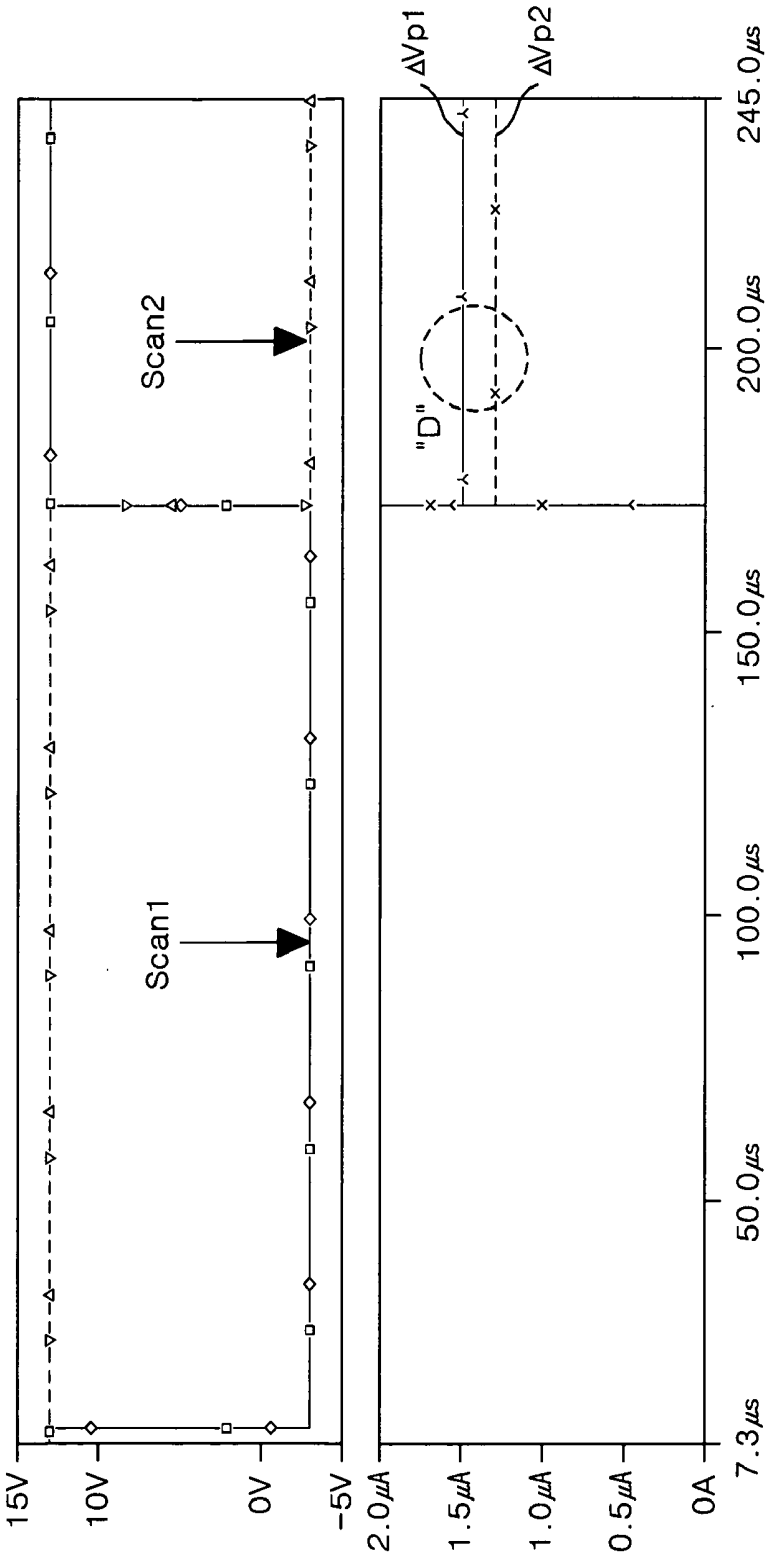


FIG.5

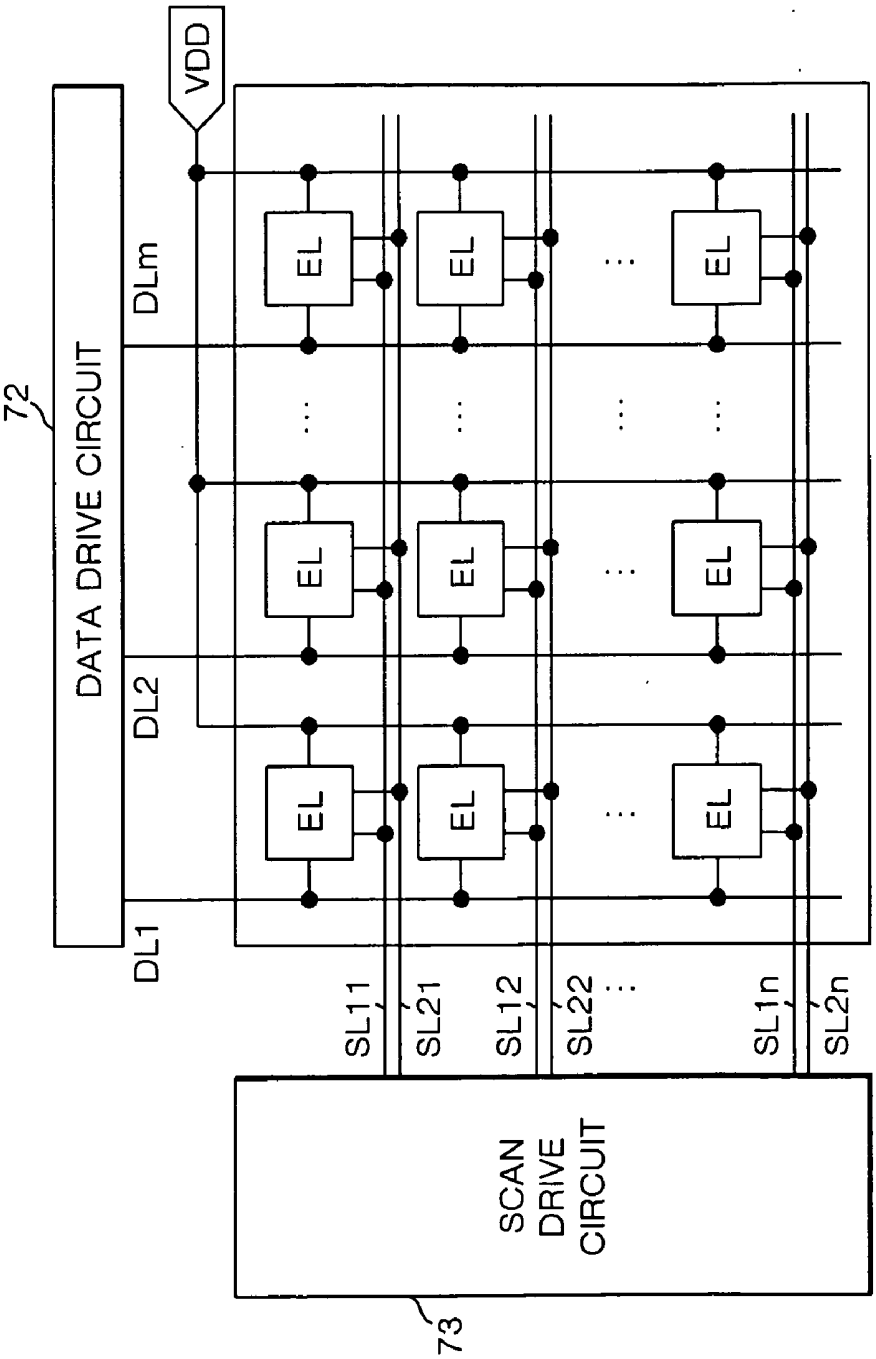

VDD
DATA DRIVE CIRCUIT
72
DLm
DL2
DL1
EL
SL11
SL21
SL12
SL22
SL1n
SL2n
SCAN DRIVE CIRCUIT
73

FIG.6A

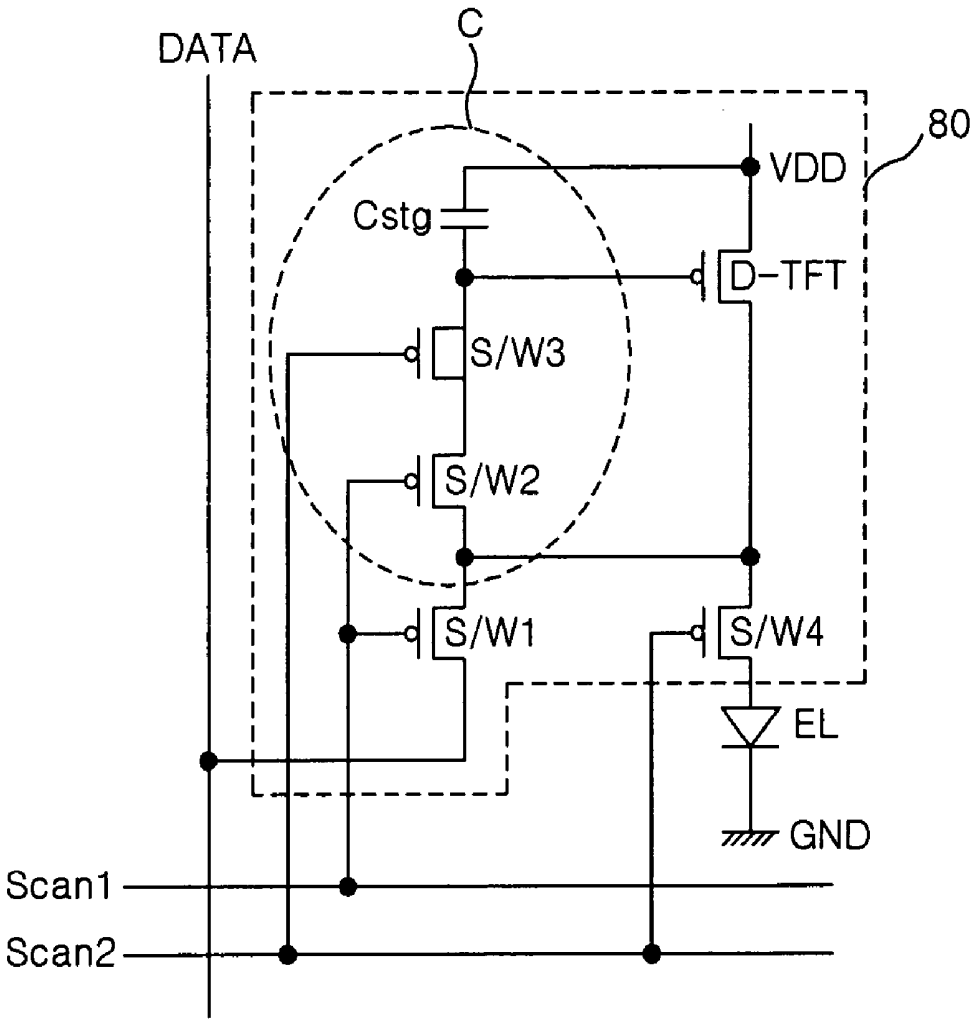


FIG.6B

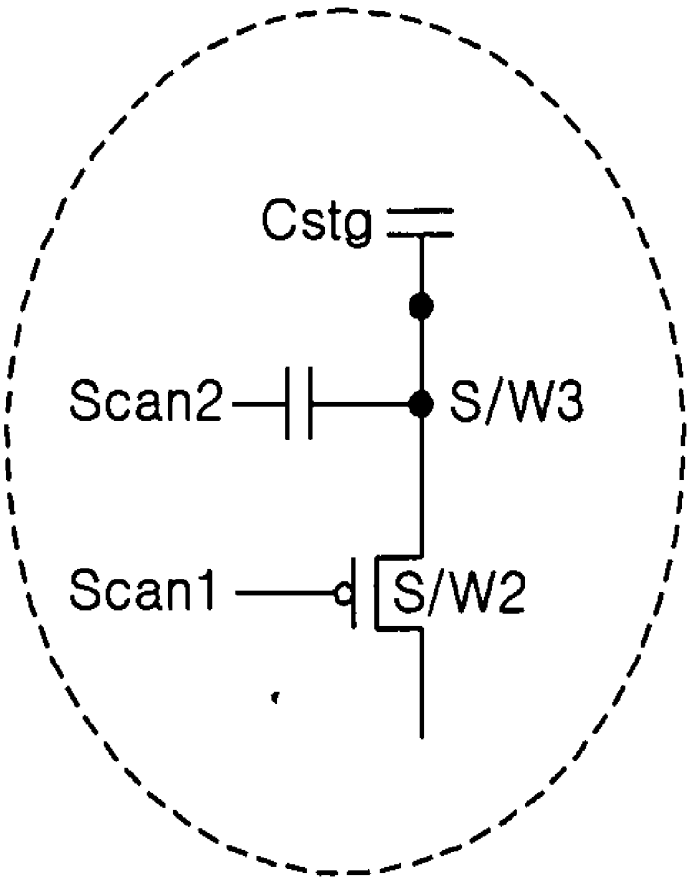


FIG.7

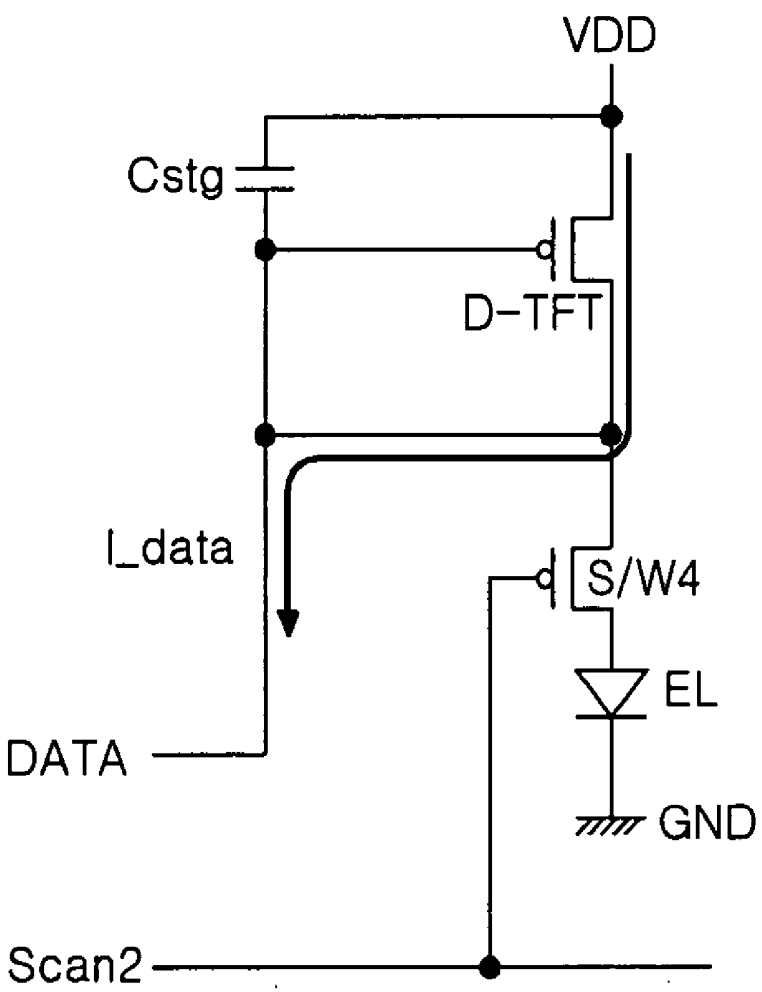


FIG.8

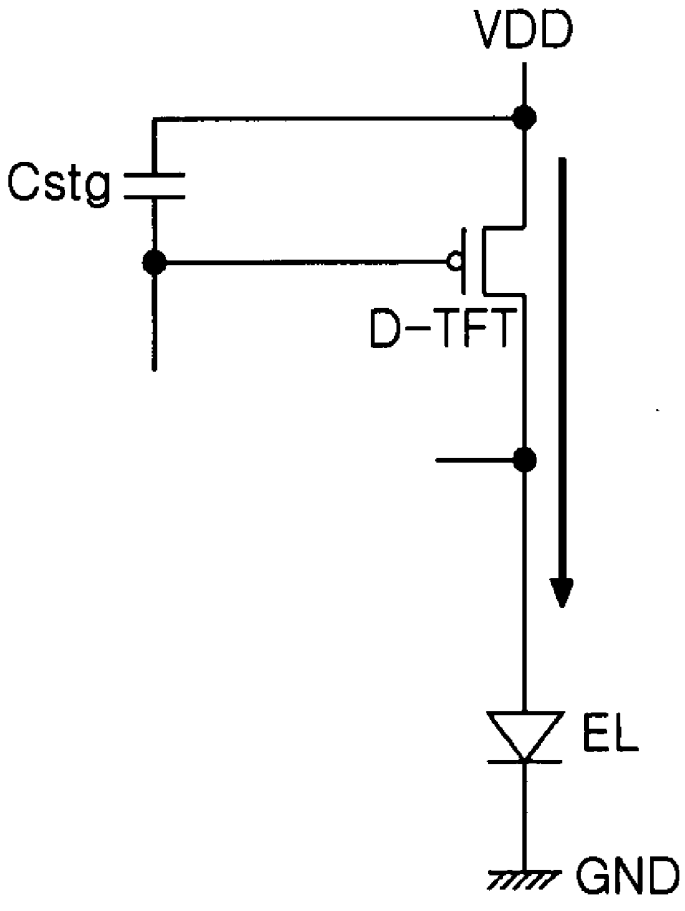


FIG.9

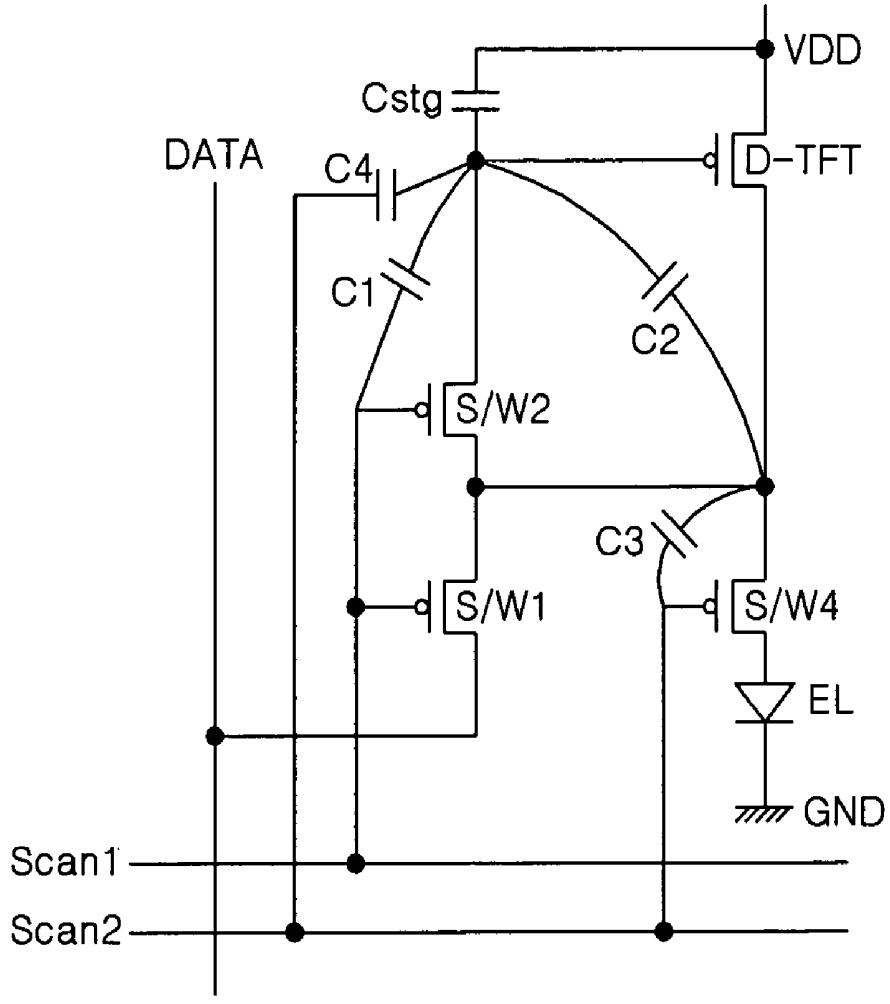
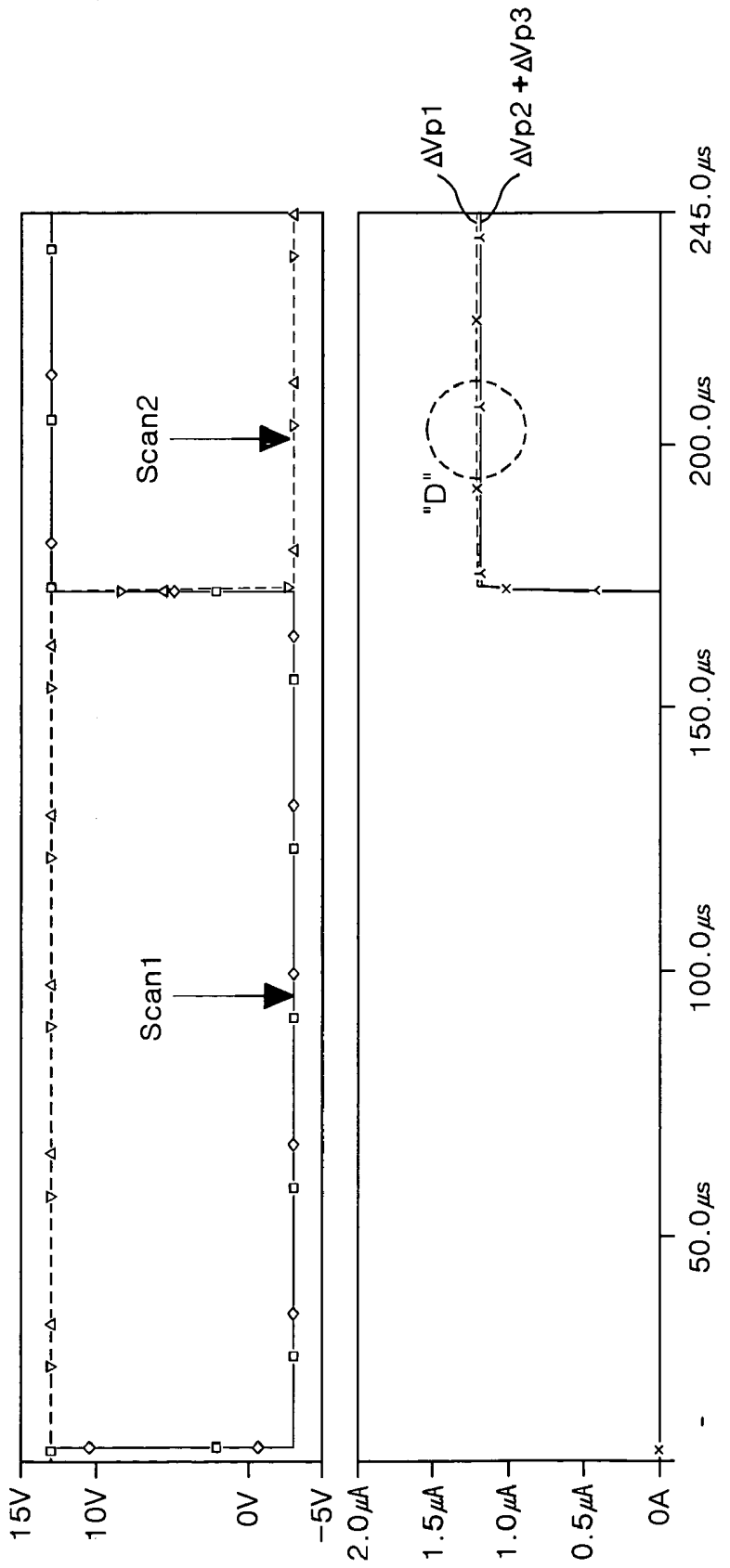


FIG.10


15V
10V
0V
−5V
Scan2
Scan1
2.0μA
1.5μA
1.0μA
0.5μA
0A
ΔVp1
ΔVp2 + ΔVp3
"D"
50.0μs
100.0μs
150.0μs
200.0μs
245.0μs

ELECTRO-LUMINESCENCE DISPLAY DEVICE AND DRIVING METHOD THEREOF

[0001] This application claims the benefit of the Korean Patent Application No. P2004-79539 filed on Oct. 6, 2004, which is hereby incorporated by reference.

BACKGROUND

[0002] 1. Field of the Invention

[0003] The invention relates to an electro-luminescence display device, and more particularly, to a current-driven type electro-luminescence display device.

[0004] 2. Description of the Related Art

[0005] Various flat panel display devices having a light-weight and a compact size have replaced a cathode ray tube (CRT). The flat panel display devices include a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP), an electro-luminescence (EL) display, an organic light emitting display (OLED) and so on.

[0006] The OLED is classified into a passive matrix and an active matrix. The active matrix OLED includes a thin film transistor, whereas the passive matrix has no thin film transistor. The active matrix OLED (AMOLED) is more suitable for a display device having a large size and a high resolution. The OLED is a self-luminous display device which electrically excites a fluorescent organic compound to emit light. It operates at low voltage and is thinner than other flat display devices. Further, the OLED has excellent characteristics such as a wide viewing angle and a rapid response speed. The OLED is currently in use for various devices, such as a hand phone, a car navigation, a hand PC and etc.

[0007] **FIG. 1** is a circuit diagram illustrating a pixel structure of a current-driven type electro-luminescence display device of the related art. Referring to **FIG. 1**, the current-driven type electro-luminescence display device **100** includes an electro-luminescence ("EL"), a switch part **10** and a data line. The EL forms a pixel in accordance with the current strength. The switch part **10** includes switches S/W**1**, S/W**2** and S/W**3** and controls the current supplied to the EL. The data line DATA and first and second scan lines Scan**1**, Scan**2** supply a signal to the switch part **10**.

[0008] The first switch S/W**1** includes a drain that is connected to the data line DATA and a gate that is connected to the first scan line Scan**1**. The second switch S/W**2** has a gate that is connected to the first scan line Scan**1** and a drain that is connected to a source of the first switch S/W**1**. A storage capacitor Cstg is arranged between a high potential voltage VDD and a source of the second switch S/W**2**. A drive transistor D-TFT has a gate that is connected between the storage capacitor Cstg and the source of the second switch S/W**2** and a source that is connected to the high potential voltage VDD. The third switch S/W**3** includes a gate that is connected to the second scan line Scan**2** and the source is connected to a drain of the drive transistor D-TFT. The EL is connected between a drain of the third switch S/W**3** and a ground GND.

[0009] **FIG. 2** illustrates a drive waveform for the electro-luminescence display device **100** of **FIG. 1**. In an interval A of **FIG. 2**, a low voltage applies to the first scan line Scan**1**. The first switch S/W**1** and the second switch S/W**2** are turned on. When the first and second switches S/W**1**, S/W**2** are turned on, the drive transistor D-TFT forms a diode connection. The current sinks to the data line DATA through the drive transistor D-TFT.

[0010] In an interval B, the first and second switches S/W**1** and S/W**2** are turned-off and the drive transistor D-TFT is turned on by a storage capacitor Cstg. The third switch S/W**3** is turned on with a low voltage supplied to the second scan line Scan**2** so that a current corresponding to a designated data value flows in the EL for one frame period.

[0011] **FIG. 3** illustrates parasitic capacitors which are hidden in the electro-luminescence display device **100**. A first parasitic capacitor C**1** is formed between the gate and source of the second switch S/W**2**. A second parasitic capacitor is formed between the source of the second switch S/W**2** and the source of the third switch S/W**3**. A third parasitic capacitor C**3** is formed between the gate and the source of the third switch S/W**3**. Due to the influence of the parasitic capacitors C**1**, C**2** and C**3**, when the first switch and the second switch S/W**1**, S/W**2** are turned off, a DC voltage offset is generated and a kickback effect occurs. The kick-back effect occurs in particular where the first and second switches S/W**1**, S/W**2** are turned off and the third switch S/W**3** is turned on.

[0012] Referring to **FIG. 4**, a kickback voltage develops in the first parasitic capacitor C**1** by as much as ΔVp**1** in a direction of increasing the gate voltage of the drive transistor D-TFT. A kickback voltage also develops in the third parasitic capacitor C**3** by as much as ΔVp**2** in a direction of decreasing the gate voltage of the drive transistor D-TFT. As a result, the kickback voltage may not be entirely cancelled and a voltage difference by "D" is generated. The voltages ΔVp**1** and ΔVp**2** are computed with the following equation (2):

$$\Delta Vp1 = \frac{C1}{C1 + C2 + C3 + Cstg} \times \Delta Vgs1 \qquad \text{(Equation 1)}$$

$$\Delta Vp2 = \frac{C2 + C3}{C1 + C2 + C3 + Cstg} \times \Delta Vgs3 \qquad \text{(Equation 2)}$$

where ΔVgs**1** is a change amount of a threshold voltage between the gate and the source of the first switch S/W**1**, and ΔVgs**3** is a change amount of a threshold voltage between the gate and the source of the third switch S/W**3**.

[0013] The kickback effect may result in a non-uniformity of a picture quality. A displayed picture appears inconsistent and uneven in accordance with its characteristics. Accordingly, there is a need of a current-driven type electro-luminescence display device which provides an improved uniformity of a picture quality.

SUMMARY OF THE INVENTION

[0014] By way of introduction only, an electro-luminescence display device includes a plurality of column lines, a plurality of first row lines, and a plurality of second row lines. The plurality of first row lines intersect the column lines and a first scan signal is supplied thereto. The plurality of second row lines intersects the column lines and a second scan signal is supplied thereto. The second scan signal is later than the first scan signal. Organic light emitting devices

are formed at pixel areas. The pixel areas are defined by the column lines and the first and second row lines. The electro-luminescence display device includes at least two drive switches and a compensation circuit which operates to be complementary to each other with the drive switch. The compensation circuit operates to compensate a kickback voltage generated upon a voltage change of the first row line. In one embodiment, the compensation circuit operates to generate an offset kickback voltage upon a voltage change of the second row line.

[0015] A driving method of an electro-luminescence display device includes installing a kickback compensation circuit adjacent a drive switches, and compensating a kickback voltage which is generated upon a voltage change of the first row line by use of the kickback compensation circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The following detailed description of the embodiments reference the accompanying drawings, in which:

[0017] **FIG. 1** is a circuit diagram representing a pixel area of a related art current-driven type electro-luminescence display device;

[0018] **FIG. 2** illustrates a drive waveform for the electro-luminescence display device of **FIG. 1**;

[0019] **FIG. 3** illustrates parasitic capacitors in the electro-luminescence display device of **FIG. 1**;

[0020] **FIG. 4** is a chart illustrating a voltage change in connection with the electro-luminescence display device of **FIG. 3**;

[0021] **FIG. 5** is a block diagram of a current-driven type electro-luminescence display device;

[0022] **FIGS. 6A and 6B** are circuit diagrams representing a pixel structure in the electro-luminescence display device of **FIG. 5**;

[0023] **FIG. 7** illustrates a signal flow via a first scan line;

[0024] **FIG. 8** illustrates a signal flow via a second scan line;

[0025] **FIG. 9** illustrates parasitic capacitors in connection with the pixel structure of **FIG. 6A**; and

[0026] **FIG. 10** illustrates a voltage change amount in connection with the parasitic capacitors of **FIG. 9**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0027] **FIG. 5** is a block diagram illustrating a current-driven type electro-luminescence display device **500**. Referring to **FIG. 5**, the current-driven type electro-luminescence display device **500** includes m×n numbers of pixels which are arranged in a matrix pattern. A pixel area is formed between m numbers of data lines DL**1** to DLm and n numbers of first and second scan lines Scan**11** to Scan**1***n* and second scan lines Scan**21** to Scan**2***n*. A data drive circuit **72** supplies a data to the data lines DL**1** to DLm and a scan drive circuit **73** sequentially supplies a scan signal to the first and second scan lines Scan**11** to Scan**1***n*, Scan**21** to Scan**2***n*.

[0028] A pixel structure of the current-driven type electro-luminescence display device **500** will be described in detail in conjunction with **FIGS. 6A and 6B**. Referring to **FIG. 6A**, the pixel structure includes a data line DL, first and second scan lines Scan**1** and Scan**2** and a drive switch **80** to drive pixels. The drive switch **80** includes a storage capacitor Cstg.

[0029] The drive switch **80** includes a first switch S/W**1**, a second switch S/W**2**, a third switch S/W**3**, a fourth switch S/W**4** and a storage capacitor. In the first switch S/W**1**, a drain is connected to the data line DL and a gate is connected to the first scan line Scan**1**. In the second switch S/W**2**, a gate is connected to the first scan line Scan**1** and a drain is connected to a source of the first switch S/W**1**. In the third switch S/W**3**, a gate is connected to the second scan line Scan**2** and a drain is connected to the source of the second switch S/W**2**. The storage capacitor Cstg is arranged between a high potential voltage VDD and a source of the third switch S/W**3**. The drive switch **80** includes a drive transistor D-TFT of which a gate is connected between the storage capacitor Cstg and the source of the third switch S/W**3**. A source of the drive transistor D-TFT is connected to the high potential voltage VDD. The driver switch **80** further includes a fourth switch S/W**4** of which a gate is connected to the second scan line Scan**2** and a source is connected to the drain of the drive transistor D-TFT. An EL is connected between a drain of the fourth switch S/W**4** and a ground GND. The source and the drain of the third switch S/W**3** are connected to each other. With that arrangement, the third switch S/W**3** may be equivalent to a capacitor as shown in **FIG. 6B**.

[0030] The drive transistor D-TFT operates in a self compensation method which compensates a voltage by itself with the storage capacitor Cstg. The storage capacitor Cstg is connected between the gate and the source of the transistor D-TFT. Accordingly, in the current-driven type electro-luminescence display device **500**, a current corresponding to a designated data value equally flows in each EL regardless of the characteristics change of the drive transistor device of an adjacent pixel. Further, such data value is sustained for one frame period after the first and second switches S/W**1**, S/W**2** are turned off by charging a data voltage in the storage capacitor Cstg.

[0031] A driving method of the current-driven type electro-luminescence display device will be described in conjunction with **FIGS. 6A** to **8**. As noted above, **FIG. 2** illustrates the drive waveform for use with the electro-luminescence display device. In the A period, the high potential voltage VDD applies to the first scan line Scan**1**. The first and second switches S/W**1**, S/W**2** are turned on as shown in **FIG. 7**. At this time, a high potential voltage VDD is charged in the storage capacitor Cstg and a current subsequently flows through a path formed by the first and second switches S/W**1** and S/W**2**. The voltage sinks at the data line through the first switch S/W**1** via the drive transistor D-TFT by as much as the potential difference between the high potential voltage VDD and the voltage which remains in the storage capacitor Cstg. For example, electric charge stored in the storage capacitor Cstg is 2V and the high potential voltage VDD is 10V The remaining voltage, i.e., 8V flows through the drive transistor D-TFT and the voltage sinks to the data line through the first switch S/W**1**.

[0032] In the B period, the high potential voltage VDD flows in the EL through the fourth switch S/W4 as shown in **FIG. 8** and at this moment, the designated current activates the EL for operation. While the voltage supplied to the first scan line Scan1 is changed from a low voltage to a high voltage, the voltage supplied to the second scan line Scan2 is changed from the high voltage to the low voltage. Accordingly, the first and second switches S/W1, S/W2 are turned off and the third and fourth switches S/W3, S/W4 are turned on. The second scan signal operates to activate the drive switch later than the first scan signal. The high, potential voltage VDD is supplied to the EL through the drive transistor D-TFT via the fourth switch S/W4 for a period except for the A period within one frame period. The designated current flows in the EL from the high potential voltage VDD.

[0033] **FIG. 9** illustrates parasitic capacitors of the current-driven type electro-luminescence display device. Referring to **FIG. 9**, the parasitic capacitors includes a first parasitic capacitor C1, a second parasitic capacitor C2, a third parasitic capacitor C3 and a fourth parasitic capacitor C4. The first parasitic capacitor C1 is formed between the gate and the source of the second switch S/W2. The second parasitic capacitor C2 is formed between the source of the second switch S/W2 and the source of the fourth switch S/W4. The third parasitic capacitor C3 is formed between the source of the second switch S/W2 and the second scan line Scan2. A fourth parasitic capacitor C4 is formed between the gate and the source of the fourth switch S/W4.

[0034] When the first and second switches S/W1, S/W2 are turned off, a kickback effect is generated by the first parasitic capacitor C1 in a direction of increasing the gate voltage of the drive transistor D-TFT. This kickback effect cancels off another kickback effect which is generated by the third and fourth parasitic capacitors C3, C4 in a direction of decreasing the gate voltage of the drive transistor D-TFT as a whole. The kickback voltage is generated in the first parasitic capacitor C1 by as much as ΔVp1 in a direction of increasing the gate voltage of the drive transistor D-TFT. The kickback voltage is also generated in the third parasitic capacitor C3 by as much as ΔVp3 in a direction of decreasing the gate voltage of the drive transistor D-TFT. Further, the kickback voltage occurs in the fourth parasitic capacitor C4 by as much as ΔVp4 in a direction of decreasing the gate voltage of the drive transistor D-TFT. The kickback voltage is cancelled off as a whole, as shown in **FIG. 10**. The third switch S/W3 may be determined to be a value that may cancel off the kickback effect which is generated with the first and second switches S/W1, S/W2.

[0035] The kickback voltage represented by ΔVp1, ΔVp3 and ΔVp4 are computed with the following equations:

$$\Delta Vp1 = \frac{C1}{C1 + C2 + C3 + C4 + Cstg} \times \Delta Vgs1 \quad \text{(Equation 3)}$$

$$\Delta Vp3 = \frac{C3}{C1 + C2 + C3 + C4 + Cstg} \times \Delta Vgs3 \quad \text{(Equation 4)}$$

$$\Delta Vp4 = \frac{C2 + C4}{C1 + C2 + C3 + C4 + Cstg} \times \Delta Vgs4 \quad \text{(Equation 5)}$$

wherein ΔVgs1 is a change amount of a threshold voltage between the gate and the source of the first switch S/W1, ΔVgs3 is a change amount of a threshold voltage between the gate and the source of the third switch S/W3, and ΔVgs4 is a change amount of a threshold voltage between the gate and the source of the fourth switch S/W4.

[0036] As described above, the current-driven type electro-luminescence display device may prevent the kickback effect of various sizes. Accordingly, the current supplied to the EL may be uniform and the picture quality defect may be prevented. As a result, an overall picture quality may substantially improve.

[0037] Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

What is claimed is:

1. An electro-luminescence display device, comprising:

a plurality of column lines;

a plurality of first row lines intersecting the column lines and receiving a first scan signal;

a plurality of second row lines intersecting the column lines and receiving a second scan signal;

an organic light emitting device formed at pixel areas, the pixel areas defined by the plurality of the column lines and the plurality of the first and second row lines;

a drive switch operable to drive the organic light emitting device; and

a compensation circuit operable to cancel a kickback voltage generated upon a voltage change of the first row line,

wherein the second scan signal operates to activate the drive switch later than the first scan signal.

2. The electro-luminescence display device according to claim 1, wherein the compensation circuit operates to generate an offset kickback voltage upon a voltage change of the second row line.

3. The electro-luminescence display device according to claim 1, wherein the drive switch comprises at least two switches operable to be turned on with the first scan signal.

4. The electro-luminescence display device according to claim 3, wherein the drive switch further comprises a third switch operable to be turned on with the second scan signal.

5. The electro-luminescence display device according to claim 4, wherein the drive switch comprises a drive transistor having a source terminal connected to a high potential voltage and the third switch supplies a voltage from the drive transistor to the organic light emitting device.

6. The electro-luminescence display device according to claim 5, wherein upon turn-on of the two switches with the first scan signal, the plurality of column lines operates as a voltage sink from the drive transistor.

7. The electro-luminescence display device according to claim 5, wherein the compensation circuit is arranged

among the second row line, a source of the second switch and a gate of the drive transistor to compensate the kickback voltage.

8. The electro-luminescence display device according to claim 1, wherein the compensation circuit comprises a switch having a source terminal and a drain terminal connected to each other.

9. The electro-luminescence display device according to claim 5, wherein the drive transistor is configured to couple to a storage capacitor at a gate terminal and a source terminal thereof and the drive transistor self-compensates a voltage with the capacitor.

10. A method for producing an electro-luminescence display device, comprising:

supplying a column line operating as a data line;

arranging a first row line and a second row line to intersect with the column line wherein the first row line and the second row line operate as a scan line;

forming a pixel area defined with the column line, the first row line and the second row line wherein the pixel area comprises an organic light emitting device;

connecting a plurality of drive switches to the column line, the first row line and the second row line wherein the plurality of drive switches operate to drive the organic light emitting device; and

supplying a compensation circuit between the second row line and the plurality of drive switches.

11. The method of claim 10, wherein supplying the compensation circuit comprises forming the compensation circuit with a transistor having a gate, a drain and a source.

12. The method of claim 11, further comprising:

coupling the drain and the source of the compensation circuit with each other and connecting the gate to the second row line.

13. A driving method of an electro-luminescence display device, comprising:

applying a first scan signal to a first switch and a second switch;

applying a second scan signal to a third switch and a fourth switch;

activating the third switch and the fourth switch later than the first switch and the second switch;

supplying a high potential voltage to a drive transistor;

canceling a kickback voltage generated upon a voltage change of the first scan signal; and

activating an organic light emitting device with application of the second scan signal.

14. The driving method of claim 13, further comprising:

generating a first kickback voltage in a direction of increasing a gate voltage of the drive transistor with the first and the second switches;

generating a second kickback voltage in a direction of decreasing the gate voltage of the drive transistor with the third and the fourth switch.

15. The driving method of claim 14, wherein canceling the kickback voltage further comprises canceling the first kickback voltage with the second kickback voltage.

16. The driving method of claim 15, further comprising determining a value for the third switch based on the kickback voltage.

17. The driving method of claim 13, further comprising:

turning on the first switch and the second switch with the first scan signal during a first interval of a frame; and

applying the high potential voltage to a data line through a path formed with the first switch and the second switch.

18. The driving method of claim 13, wherein canceling the kickback voltage comprises generating an offset kickback voltage to be complementary to the kickback voltage.

19. The driving method of claim 17, further comprising:

turning off the first switch and the second switch during a second interval of the frame; and

turning on the third switch and the fourth switch during the second interval of the frame.

20. The driving method of claim 19, further comprising:

applying the high potential voltage to the organic light emitting device through the fourth switch.

* * * * *

专利名称(译)	电致发光显示装置及其驱动方法		
公开(公告)号	US20060071883A1	公开(公告)日	2006-04-06
申请号	US11/168951	申请日	2005-06-28
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG飞利浦LCD CO.，LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO.，LTD.		
[标]发明人	OH DU HWAN		
发明人	OH, DU HWAN		
IPC分类号	G09G3/30 G09G3/32		
CPC分类号	G09G3/3233 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2320/043		
优先权	1020040079539 2004-10-06 KR		
其他公开文献	US7573443		
外部链接	Espacenet USPTO		

摘要(译)

一种电致发光显示装置，包括多条列线，多条第一行线和多条第二行线。多个第一行线与列线交叉，并且向其提供第一扫描信号。多条第二行线与列线相交，并且向其提供第二扫描信号。有机发光器件形成在由列线和第一和第二行线限定的像素区域处。至少两个驱动开关用于驱动有机发光器件。第二扫描信号晚于第一扫描信号施加以激活驱动开关。在第一行线的电压变化时产生反冲电压。反冲补偿电路用于消除反冲电压。